BALASAHEB S. DARADE

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OBJECTIVE

To obtain research position in Nano, MEMS. Extensively interested in research activities and assisting Professor in his research work with a positive commitment.

EDUCATION

- Jawaharlal Nehru Engineering College (JNEC), Aurangabad
  Dr BAM University, established in 1958, Maharashtra, India. (**Govt. of India Scholarship**)
  Bachelor of Engineering in Electronics & Telecommunication (2001-2005) A+ Distinction
- Jawahar Navodaya Vidyalaya, Basamathnagar (**Govt. of India HRD Scholarship**)
  AISSCE, CBSE (10+2) (1999-2001) A+ Distinction
  AISSE, CBSE (10) (1999) A First Class

AREAS OF INTEREST

Nanoelectronics, MEMS, Mixed Signal.

COURSES UNDERTAKEN

JNEC : VLSI, Electronic Devices and Circuits, Linear Integrated Circuits, Electronics Design Technology, Network Theory, Embedded Systems, Microprocessor, Communication Principals, Digital Electronics, Digital Signal Processing, Electromagnetic Engineering, Computer Oriented Numerical Methods, Engineering Mathematics (Four Courses).
MIT (Massachusetts Institute of Technology) Open Course Ware- 10 Courses in Microelectronics, Integrated Circuits, Micro- Nano Processing, Solid State Circuits, Devices.
National Program on Technology Enhanced Learning- 5 Courses in VLSI design, IC, Semiconductor Devices
IEEE Continuing Education Program- 2 Certificate courses in Transition into Management and Wireless.

SKILLS

VLSI CAD Tools	Agilent's ADS Momentum , Tanner EDA tool
Software tools	MATLAB, Xilinx (VHDL), Active-HDL
Operating System	Unix, Linux, Windows NT/98/XP
Languages/HDL	C, C++, Assembly x86, VHDL, JAVA, J2EE, SQL
Other Skill areas	VLSI, Analog Mixed Signal Design, VCO, RF MEMS, Nanotech

TRAINING/ WORK EXPERIENCE

- Programmer Analyst, Cognizant Technology Solutions, Pune (Feb 06- Aug 07)
- Rexcorp Nanotech – "MEMS Technical Expert". (Part time) (Nov 05 – Aug 07)
- **NASA:** Worked with NASA team at Lonar (Project Leader: Prof. Horton Newsom, Jan 2005)
  Role: Electronics and Communication related work like Mapping through GPS, Lonar Crater Study.
  Participation in and contributed to **"Deep Impact Mission-2004**", **NASA.**
  Participation in and contributed to **"MARS Exploration Rover-2003 Mission**", **NASA.**

- Semiconductor Complex Ltd., Chandigarh (SCL): (India Chip Program) Participation in Multiwafer fabrication Run, supported by Govt. of India. Two design ideas selected for fabrication, Design, Fabrication and Testing in collaboration with SCL and JNEC. (Feb 2005)
- Ambekar Associates- FPGA board development, Embedded application development. (Feb 2004- Jan 2005)
- Zoology Dept, Dr. B.A.M. University - Electro neurophysiology project. (Nov 2003 - Jan 2004)

PROJECTS

- Low Phase Noise Wideband VCO using MEMS
- Wireless Point-to-Point Digital Audio-Video-Data Terminal (Idea selected for Fabrication under India Chip Program, SCL*)
- Bandgap bias network circuit (Idea selected for Fabrication under India Chip Program, SCL*)
- Collateral Allocation Management, JPMC*(Software Project) Cognizant Technology Solutions*
- Profile Seeker, JPMC (Software Project) Cognizant Technology Solutions
- VCO for 3G/ 4G Wireless Communication, (BE Final year project) Apr 2005
- Wireless Stepper motor control-JNEC IEEE Student Project Contest. Apr 2004
- Cam less Valve Train -TECHFEST 2003, IIT Bombay. Jan 2003
- DSP-FPGA Codesign for industrial Applications Jan 2004
- Oil Temperature Controller.-State level project contest. Nov 2003

* Semiconductor Complex Ltd., Govt. of India Enterprise
* JPMC- JPMorgan Chase & Co. (NYSE: JPM) is a leading global financial services firm with assets of $1.3 trillion and operations in more than 50 countries.

ACHIEVEMENTS/ AWARDS

- **University Graduate Scholarship (UGS) 2007-08**, University of Cincinnati.
- **Outstanding Engineering Student** award, **IEEE**, 2004.
- **Outstanding Engineering Student, Dr B.A.M. University**, 2003-04.
- **Distinguished Alumni** – JNEC Aurangabad.
- Nominated for Larry K. Wilson RAB IEEE R10 Award, 2004.
- **LONAR RATNA,** Award for Scientific Contribution for development of Lonar Crater.
- **Best Paper Award** (First position) in International conference on Systematics, Cybernetics and Informatics 2007
- **Govt. of India Scholarship, 2001-2005,** Undergraduate Studies.
- **Govt. of India HRD Scholarship, 1994-2001**
- **First Prize: IMS -2005** (Indian Microelectronics Society Conference).
- **First Prize:** UG/PG Student Contest 2004, IEEE Communication Society.
- **First Prize:** Hardware/software Project Contest, VIT IEEE SB, 2005.
- Consolation prize, Open Hardware contest, IIT Bombay-TECHFEST 2003.
- Finalist in Prof. K. Shankar Project Contest, IEEE Bombay Section 2004 & 2005.
- Semifinalist - **CSIDC-2004 (IEEE Computer Society International Design Contest**). & **CSIDC 2005**, Role-Team Leader.
- Finalist at IIT Madras SHAASTRA 2003, Open Hardware, Project-X.
- First Prize: State level Technical Quest, VIIT IEEE, 2002.

PUBLICATIONS

- **Balasaheb S Darade** "Low Phase Noise Wideband VCO using MEMS", presented in 48th IEEE Midwest International Symposium on Circuits and held at Cincinnati, Ohio, **USA** 7-10 Aug 2005 (**MWSCAS 2005**), MEMS I.
- **Balasaheb S Darade**, Tarun A Parmar "Low Phase Noise Fully Integrated VCO", presented in Research Scholars Forum, 18th IEEE International Conference on VLSI Design 2005, Calcutta, 3-5 Jan 2005.
- **Sandip Dalvi** , Balasaheb S Darade "Supplier Evaluation for Part Procurement Using ISA", presented in **ICSCI-2005** (International Conference on Systematics, Cybernatics and Informatics Jan 2005), Pentagram research center, Hyderabad ,Page 534-539 Vol.1
- **Balasaheb S Darade**, Swapnil Dabhade, Sandip Dalvi "ECVAS for Camless Engine", presented in **IMAE-2005** (IEEE International conference on Multidisciplinary of Engineering), Jan 2005, IEEE Bombay Section, Page 50.
- **Balasaheb S Darade**, Tarun A Parmar "RF MEMS for Wireless Communication", presented at K-SHANKAR Paper Competition, IEEE Bombay, 2 Apr 2005.
- **Balasaheb S Darade**, Tarun A Parmar, J.G. Rana "VCO using MEMS Capacitor" presented in **IMS** (Indian Microelectronics Society Conference)-2005, 18-19 Feb 2005, Chandigarh.
- **Balasaheb S Darade**, Shrikant Bharthulwar, Abhijeet Chavan, Tarun A Parmar, Abhijeet Jadhav "Stampede Warning and Protection System for Crowded and Congested places of Social Importance", selected for IEEE Computer Society International Design Contest '04 and K-Shankar Project Competition '04, IEEE Bombay Section.
- **Balasaheb S Darade**, Abhishek Chauhan, Tarun A Parmar "Programming FPGA's using Handel- C", presented at 'SHAASTRA', IIT Madras, 10 Oct 03.
- **Balasaheb S Darade**, Divya Prakash Jha, Nipun Gupta, Satya Prakash "Emotional Transit", selected for IEEE Compute Society International Design Contest '05.
- **Anil Omanwar**, Balasaheb S Darade "Sixth Sense Tutoring System- An ITS", **ICSCI-2007** (International Conference on Systematics, Cybernatics and Informatics Jan 2007), Pentagram Research Centre, Hyderabad.

MEMBERSHIPS

- Student Member, IEEE. Chairman of JNEC IEEE Student Branch 2003-05, Founder -JNEC IEEE Students Association.
- Member of VSI (VLSI Society of India), IMS (Indian Microelectronics Society).
- IEEE Nanotechnology Council, IEEE Communication Society.
- Chairman of JNEC ISTE Student Chapter 2003-04.
- Member of International Association of Engineers (IAENG).

MISCELLANEOUS

- Delivered talks on Nanotechnology Overview, Analog Mixed signal design, IEEE Standards, Research trends in Electronics & Communication related topics in JNEC Auditorium.
- Key role in collaboration of JNEC with Semiconductor Complex Limited, for India Chip Program. JNEC Aurangabad was one of the five institutions in India along with IIT's, BITS Pilani short listed.
- Conference Paper Reviewer- IEEE International VLSI Design Conference

➢ Reference available on request.
➢ Please visit http://balasahebsdarade.googlepages.com for detailed information.

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